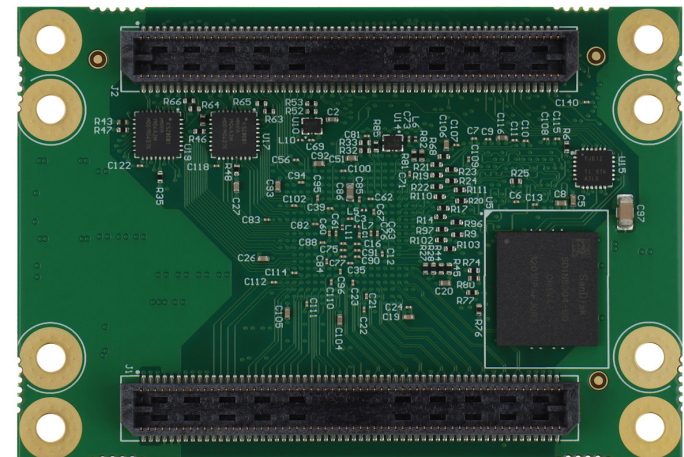
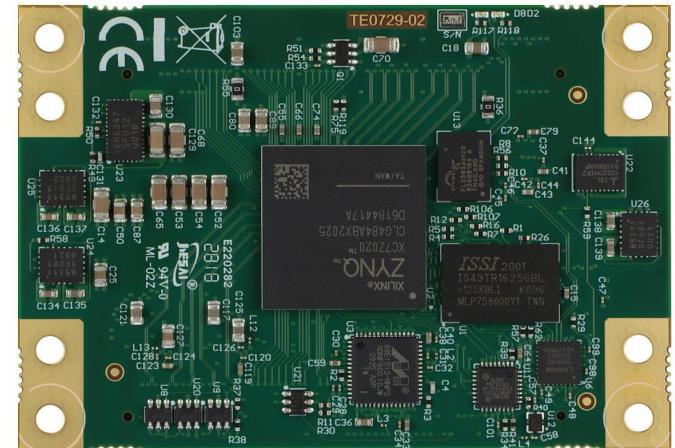
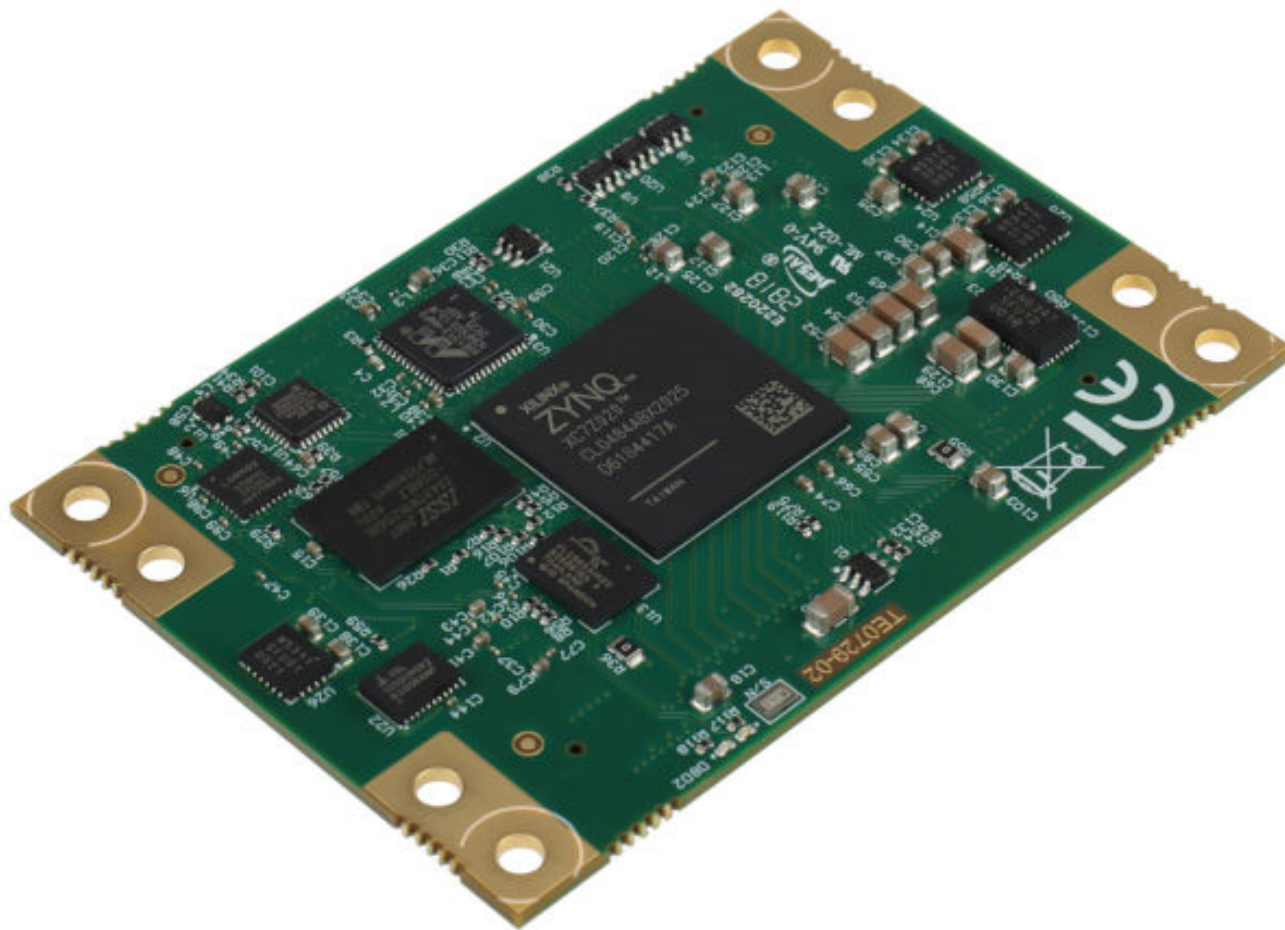




Regarding the usage of our schematics and alike documentation for Trenz module TE0729.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified.

TE0729 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TE0729 – Legal Notice		
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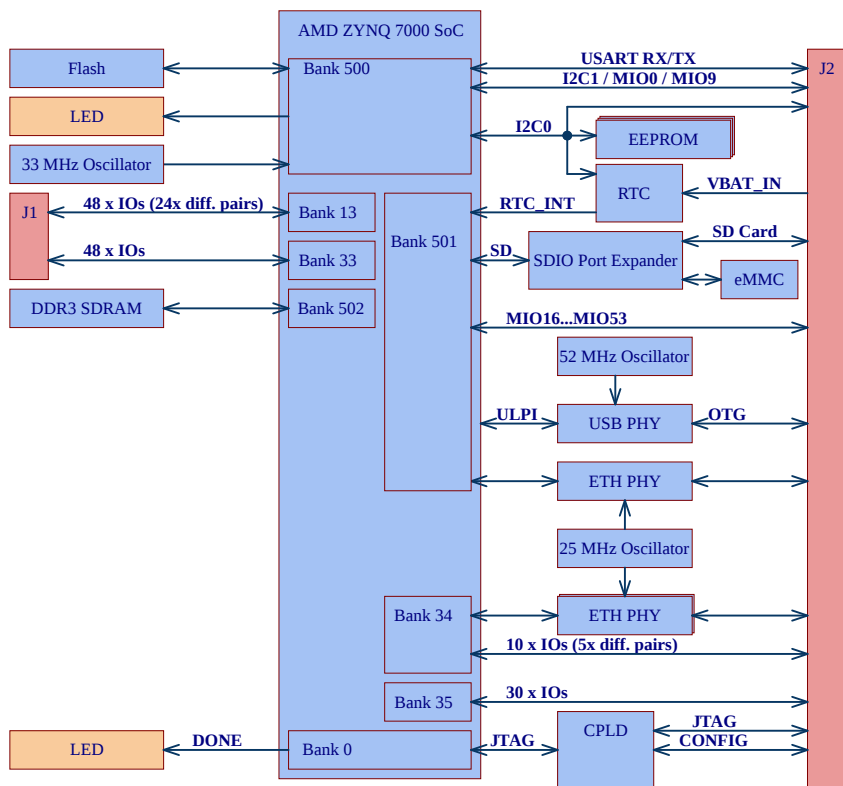
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REV	DATE	Description	
-01	-	Initial Revision	-
-02	-	-	-
-03	2023-12-01	1) Changed DCDC (U24, U25, U26) from EN5311QI to MPM3834C. 2) Changed DCDC (U23) from EN6347QI to MPM3860GQW-Z. 3) Changed load switch (Q1) from TPS27082LDDCR to MP5077GG-Z. 4) Added power supervisor (U4). 5) Changed power net name from 1.5V to DDR_VDD. 6) Changed power sequencing. 6.1) Voltage supervisor (U4) enables 1V voltage rail (DCDC U23) via signal EN_Module. 6.2) 1V DCDC (U23) enables 1.8V voltage rail (DCDC U25) via signal PG_1V0. 6.3) 1.8V DCDC (U25) enables 2.5V (DCDC U24) and DDR_VDD (DCDC U26) voltage rails via signal PG_1V8. 6.4) Voltage rail 3.3V (load switch Q1) is logical AND-enabled via 6.4.1) power good signal PG_2V5_3V3 from voltage rail 2.5V DCDC (U24) and DDR_VDD DCDC (U26) via diode (D4) 6.4.2) CPLD (U6) signal EN_3V3 via diode (D5). 7) Added level shifter in signal FPGA_IO (U7, C185, C186) to separate power domains. Added resistor R91 as fallback. 8) Added diode D3 between U21 pin 3 net nRST_in and voltage rail 3.3V. 9) Added option to improve noise immunity for signal nRST_in via capacitor C187 (default: not assembled). 10) Connected exposed pad to GND for SDIO port expander (U15). 11) Added decoupling capacitors: 11.1) C166 for U2I. 11.2) C178 for U2H. 11.3) C167 and C173 for U11. 11.4) C168... C171 for U3C. 11.5) C172 and C179 for U5B. 11.6) C174 for U15. 11.7) C175 for U8. 11.8) C176 for U9. 11.9) C177 for U20. 12) Changed 10 µF capacitors (C36, C86) to 22 µF. 13) Changed 22 µF capacitors (C117, C121, C125, and C127) from size 0805 to 0603. 14) Changed capacitor C144 from 470 nF, 6.3 V, X5R, 20 % to 100 nF, 16 V, X7R, 10 %. 15) Pulled-up board revision signal (U2D) pin H17) and added board revision documentation. 16) Changed fiducials to standard fiducials. 17) Removed serial number S/N. 18) Added testpoints TP1...TP41. 19) Added serial number box on bottom overlay. 20) Changed signal trace length. 21) Added revision history, block and power overview and additional information. Updated page count and order.	ED

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Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 V	+/- 5 %	Baseboard Power	Baseboard Power Supply.
VBAT_IN	IN	1.8 V - 5.5 V	-	Micromodule Power	Supplies RTC.
VCCIO_13	OUT	3.3 V	-	Micromodule Power	Supplied by [3.3V].
VCCIO_33	OUT	3.3 V	-	Micromodule Power	Supplied by [3.3V].
1.8V	OUT	1.8 V	-	Micromodule Power	Supplies module periphery.
2.5V	OUT	2.5 V	-	Micromodule Power	Supplies module periphery.
3.3V	OUT	3.3 V	-	Micromodule Power	Supplies module periphery.

I2C Address:

Device	I2C BUS	I2C ADDR	Note
SoC U2E	I2C0	-	Master
EEPROM U8	I2C0	0x50	-
EEPROM U9	I2C0	0x51	-
EEPROM U20	I2C0	0x52	-
RTC U22	I2C0	0x6F	-
SRAM U22	I2C0	0x57	-

Legend:

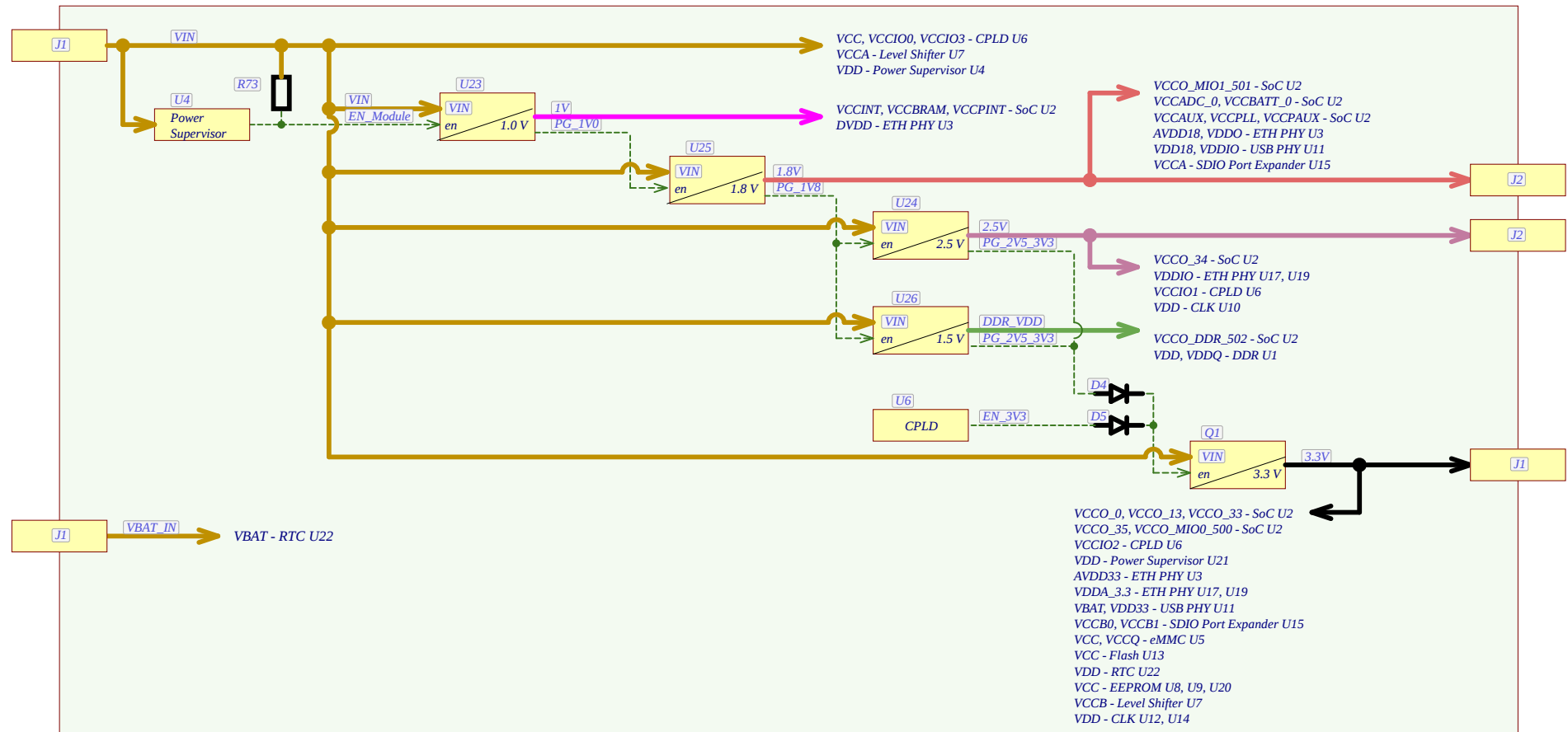
B2B Connector
 LED Interface
 On-board Components

ZYNC_POWER

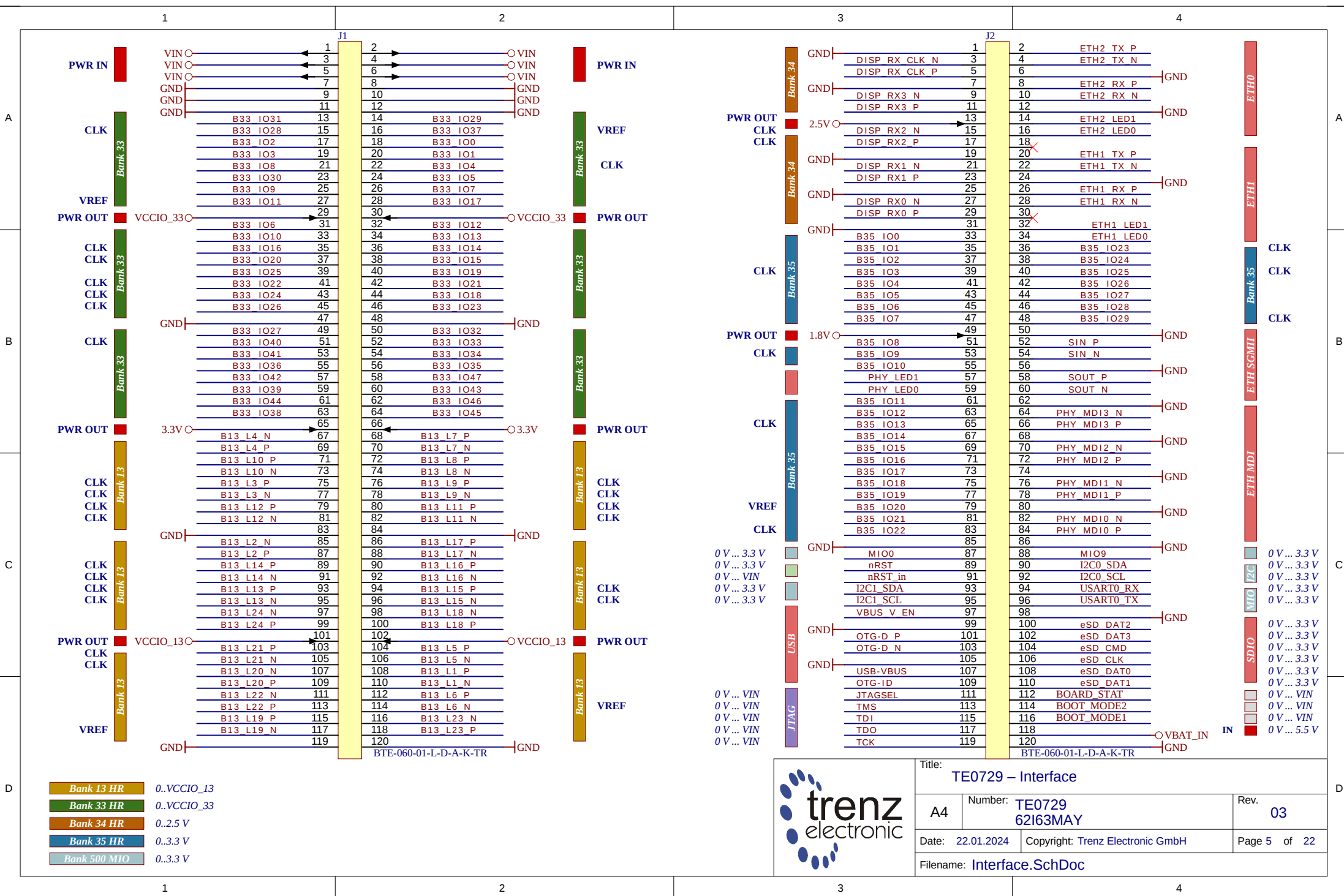
Power

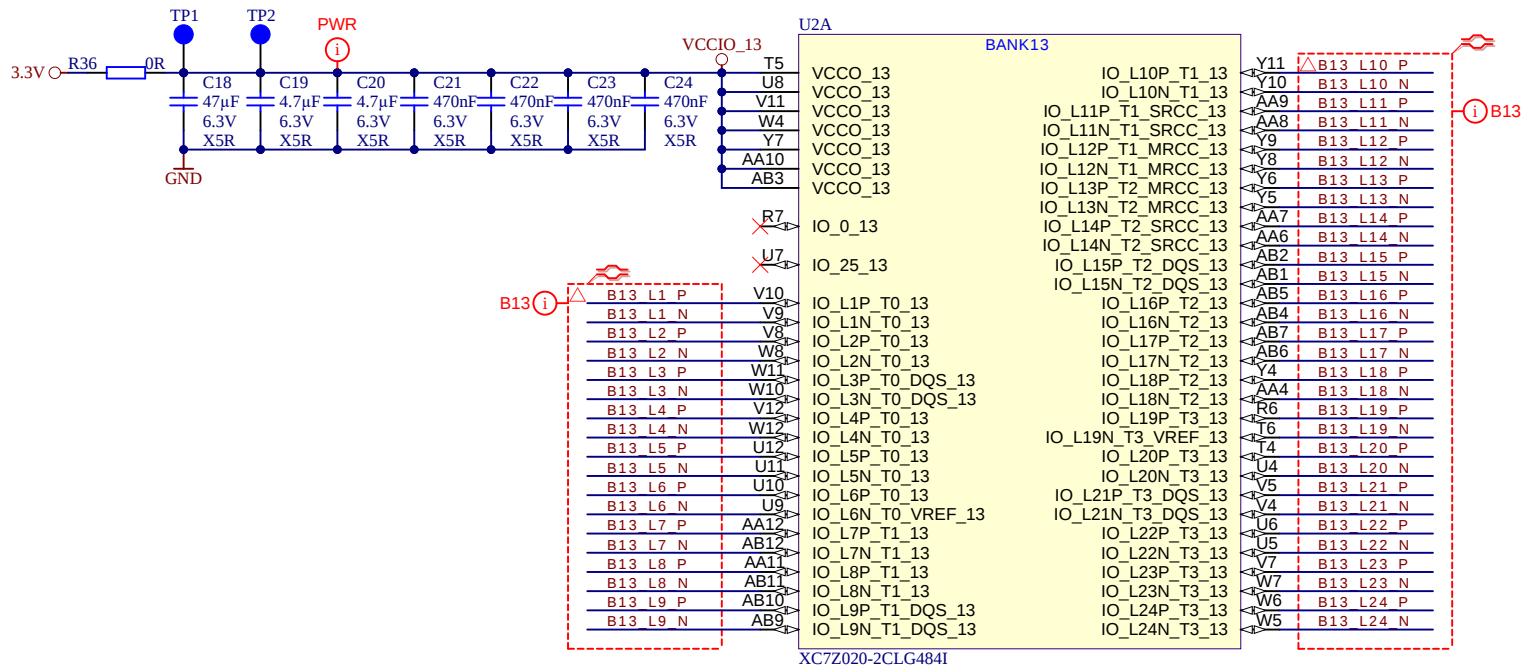


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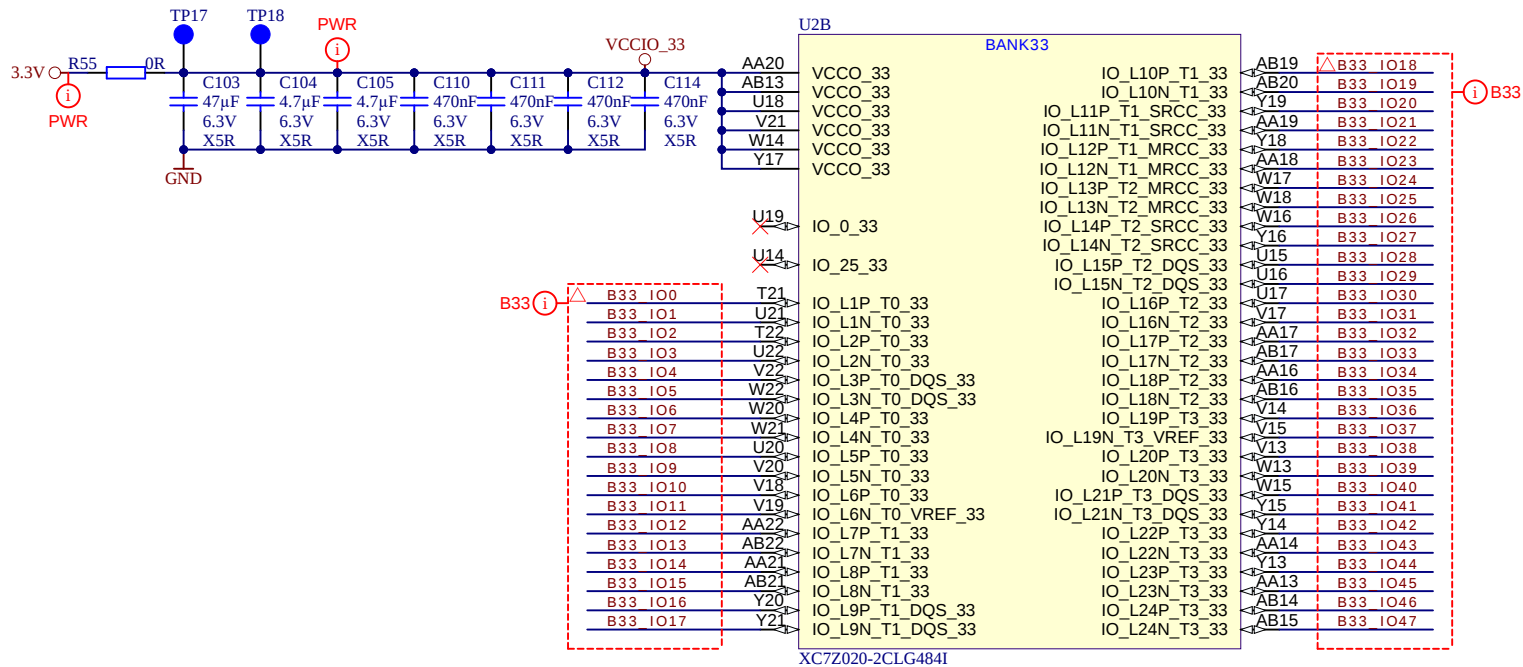


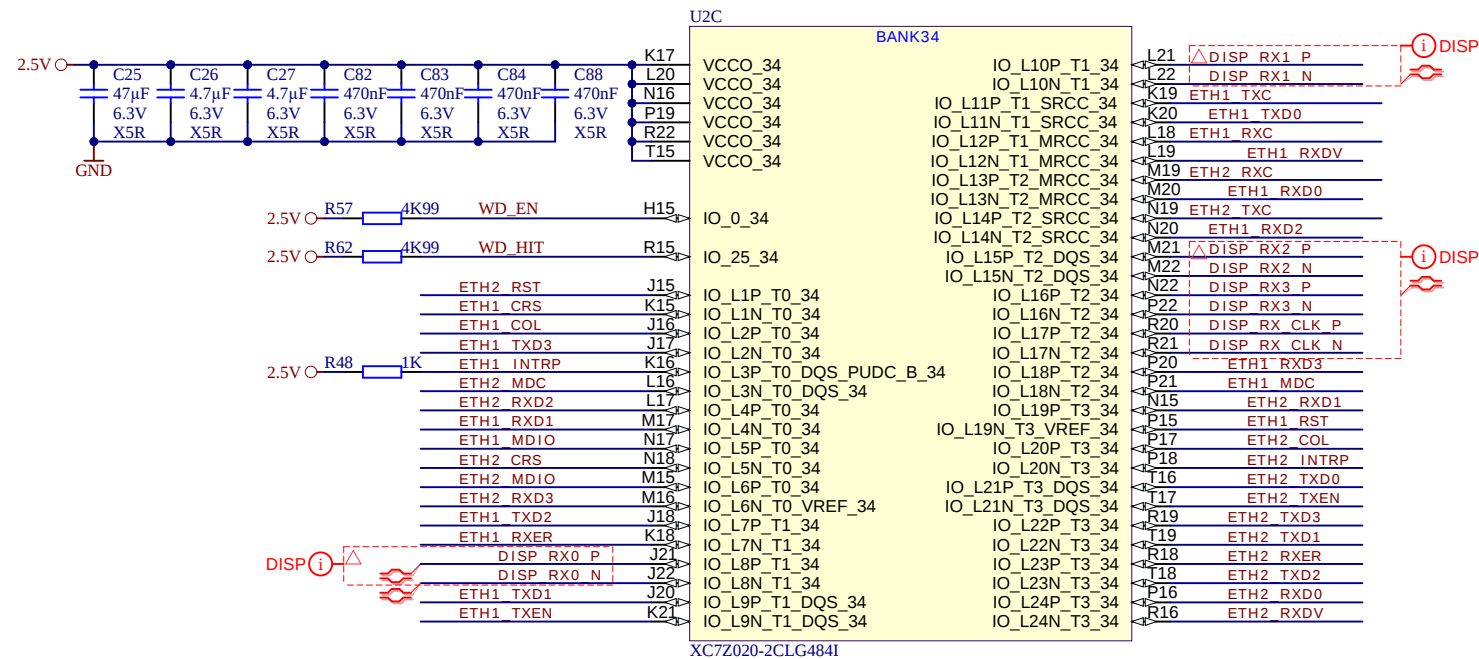
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	Date: 22.01.2024	Copyright: Trenz Electronic GmbH	Page 4 of 22
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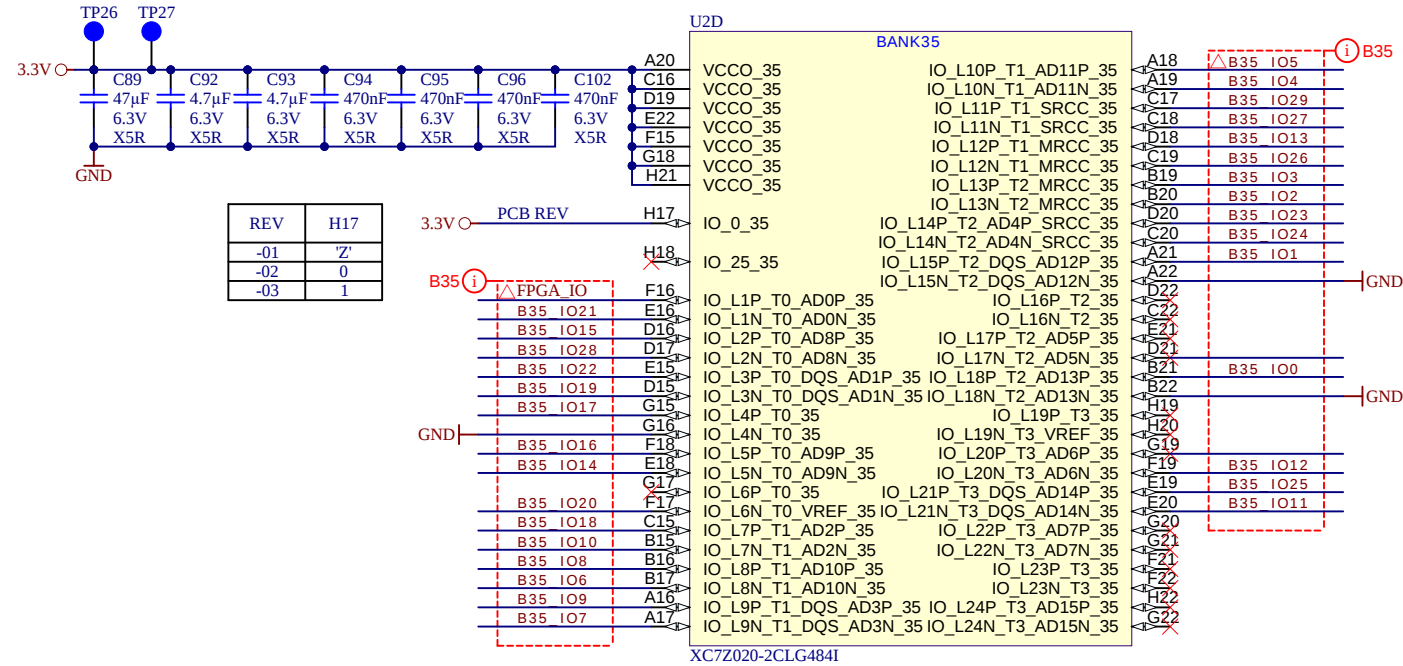


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Filename: B13.SchDoc		Page 6 of 22	
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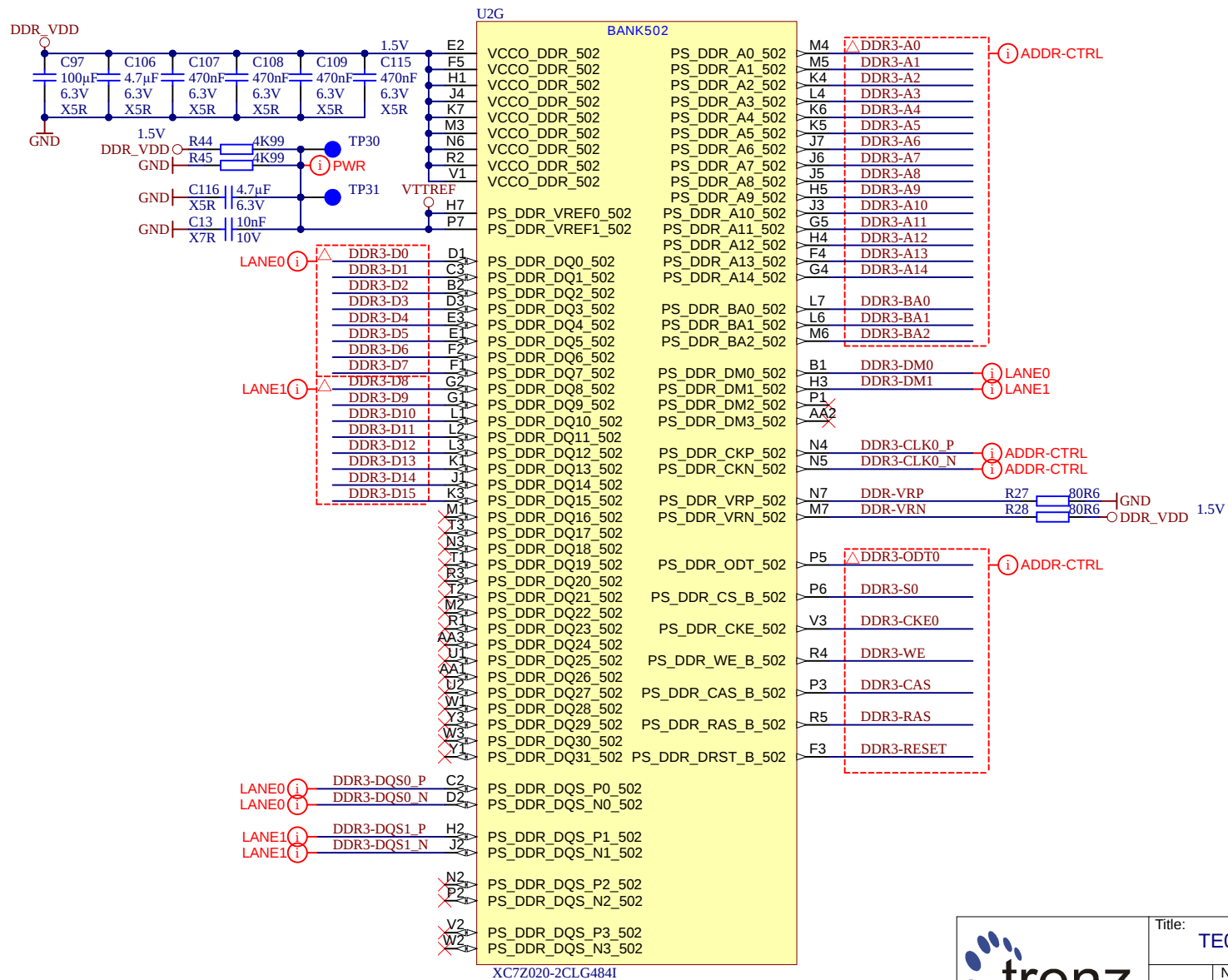




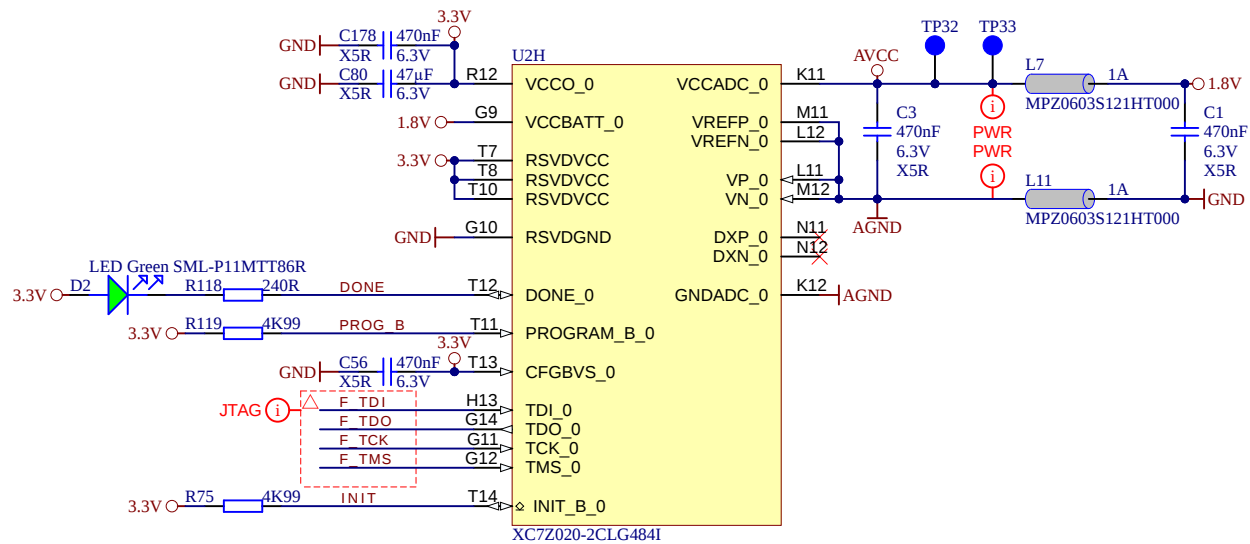
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Filename: B34.SchDoc		Page 8 of 22	



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Date: 22.01.2024		Copyright: Trenz Electronic GmbH	
Filename: PS-DDR.SchDoc		Page 12 of 22	



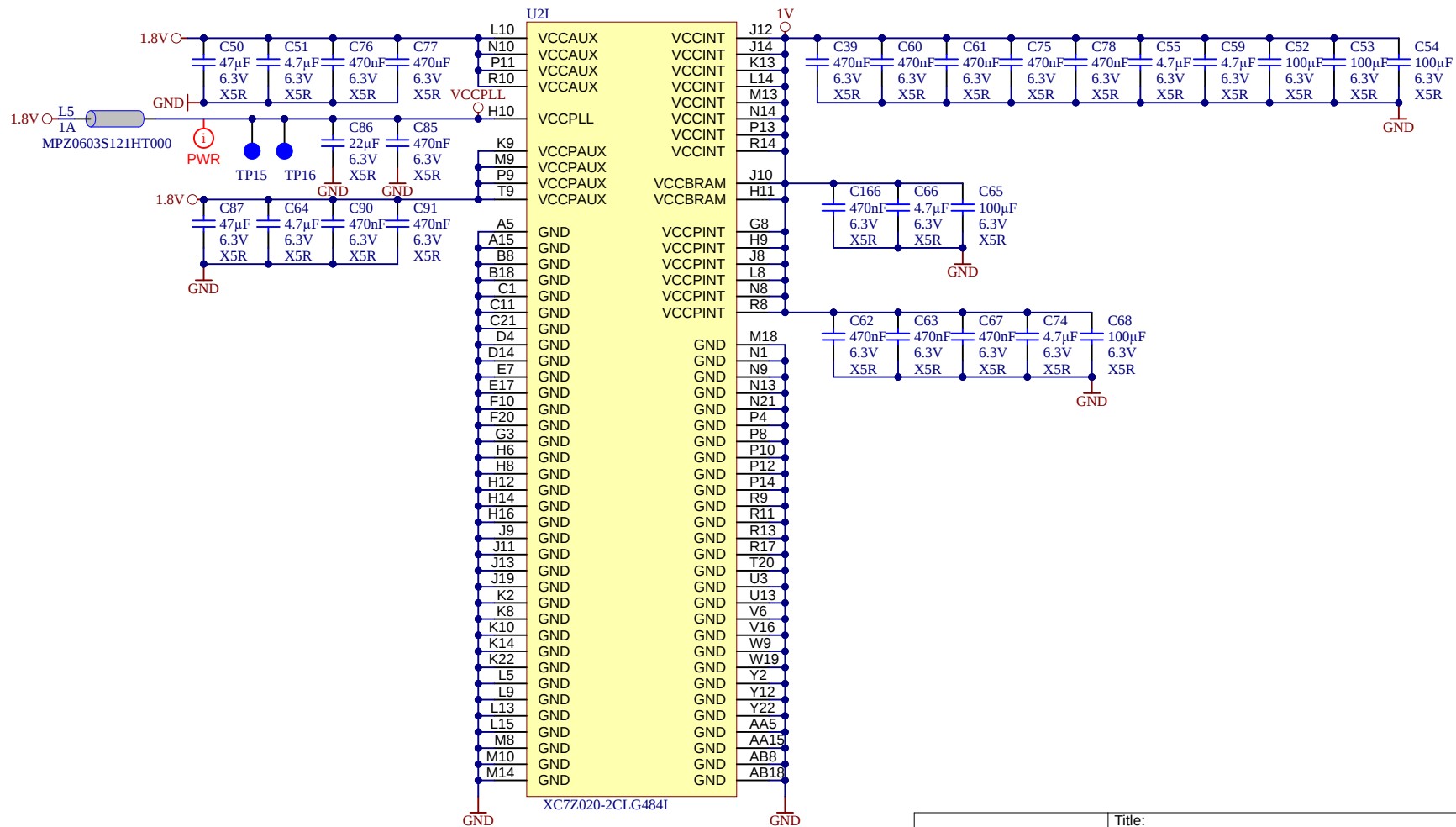
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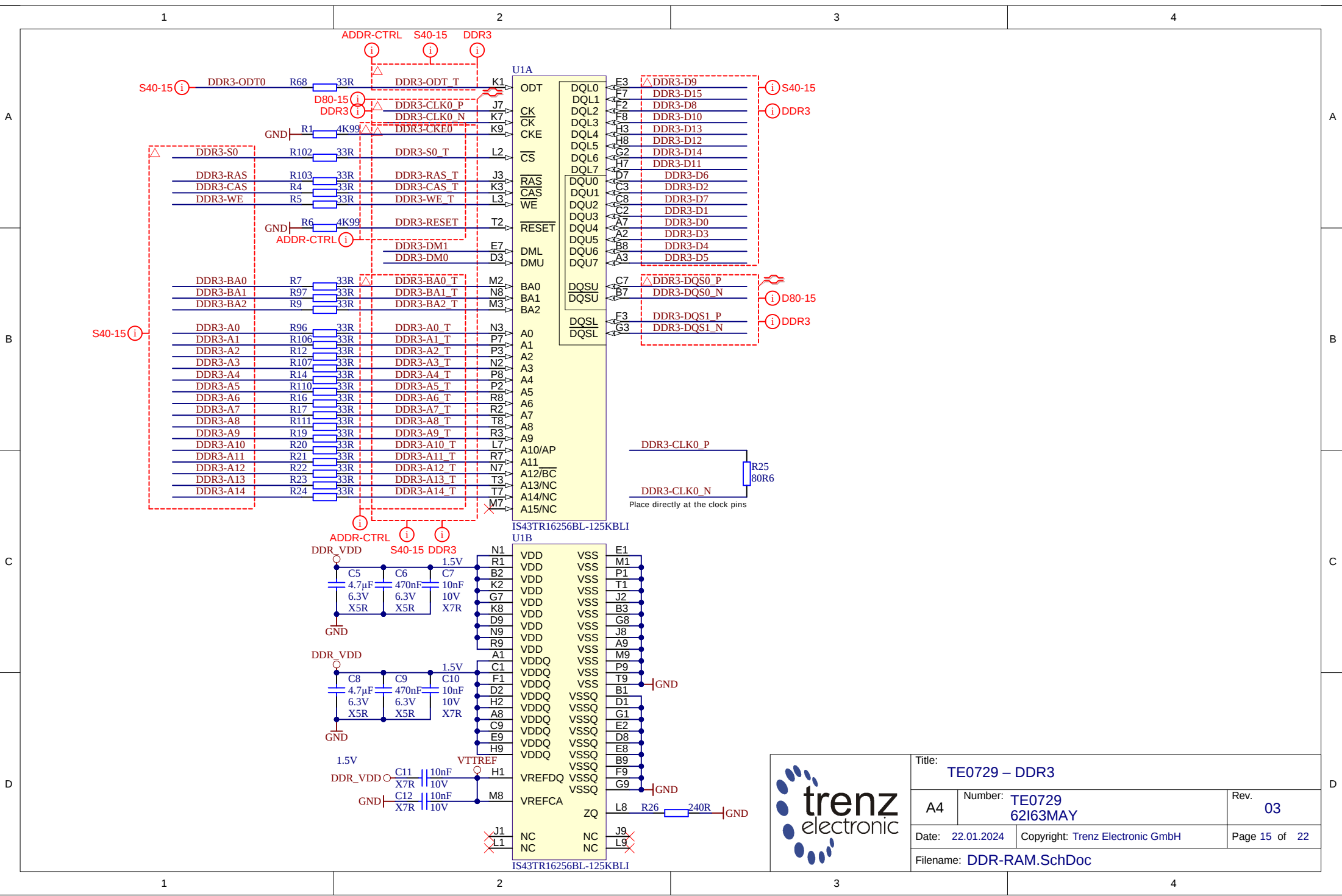
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Title: TE0729 – DDR3			
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U5D

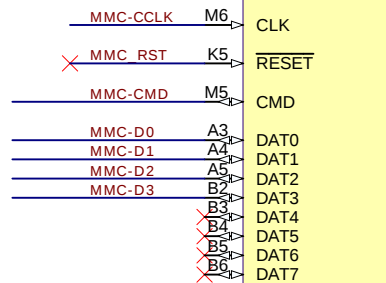
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A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M1
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

SDINBDG4-8G-XI2

MMC-D3

VDDIM

U5A



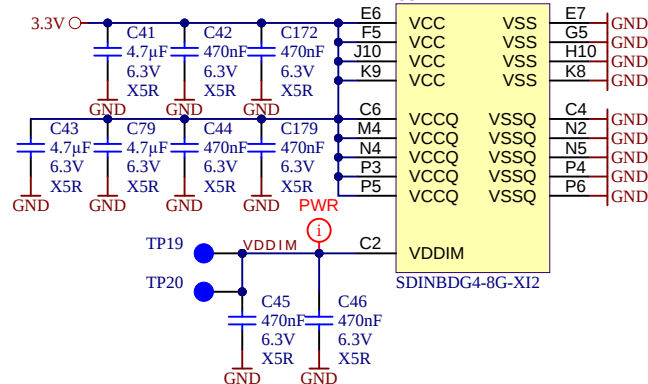
SDINBDG4-8G-XI2

U5C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
F10	RFU
F10	RFU/NC
G3	RFU
G10	RFU/NC
H5	RFU
J5	RFU/DS
K6	RFU/VSS
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

SDINBDG4-8G-XI2

U5B



SDINBDG4-8G-XI2



Title:

TE0729 – eMMC

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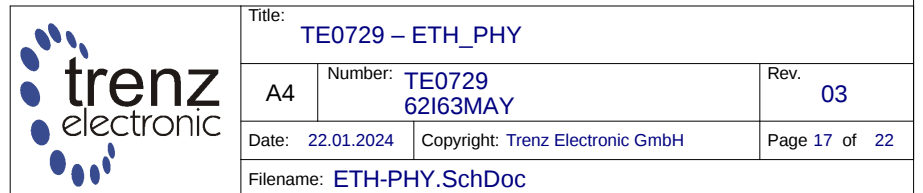
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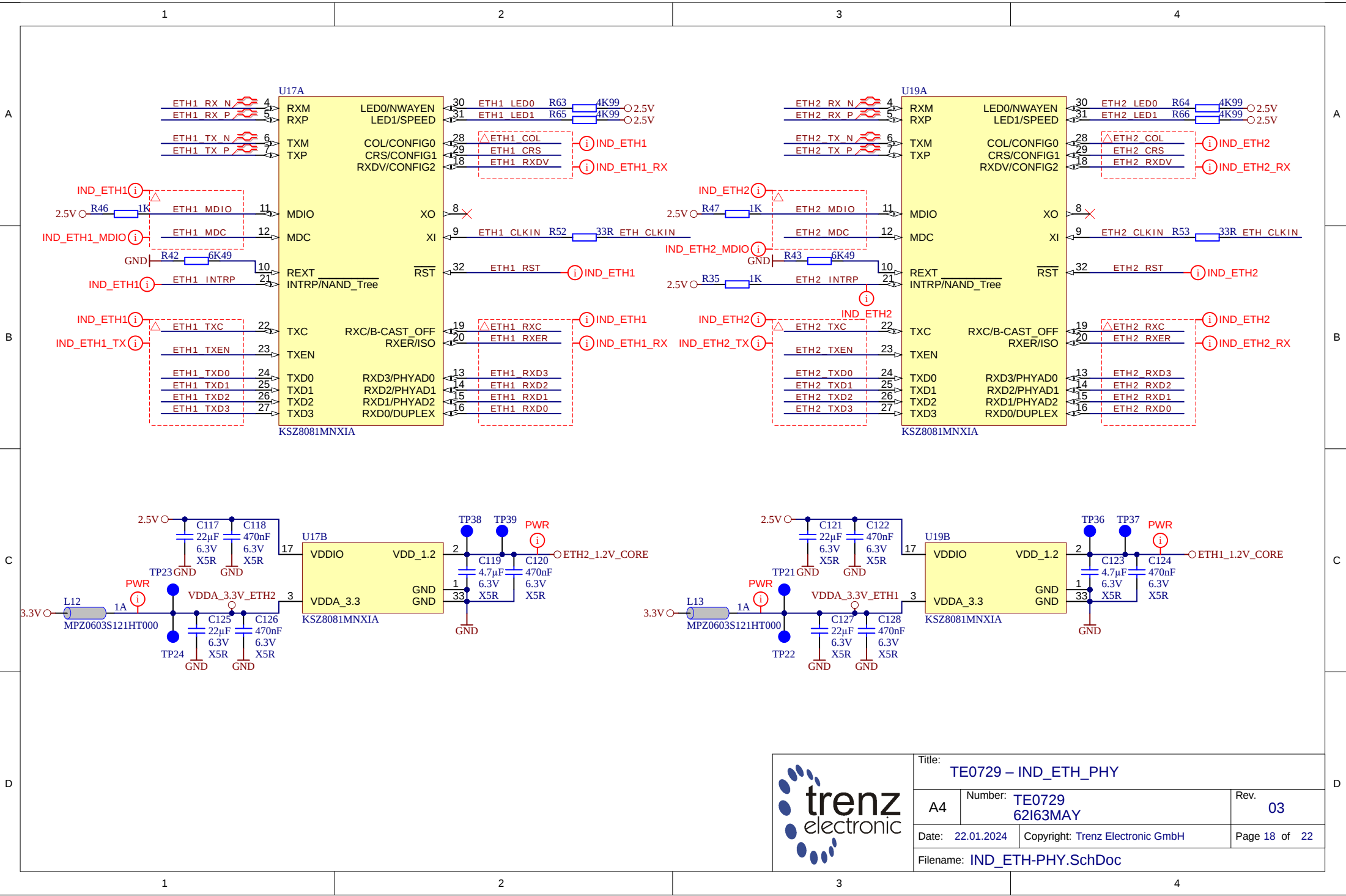
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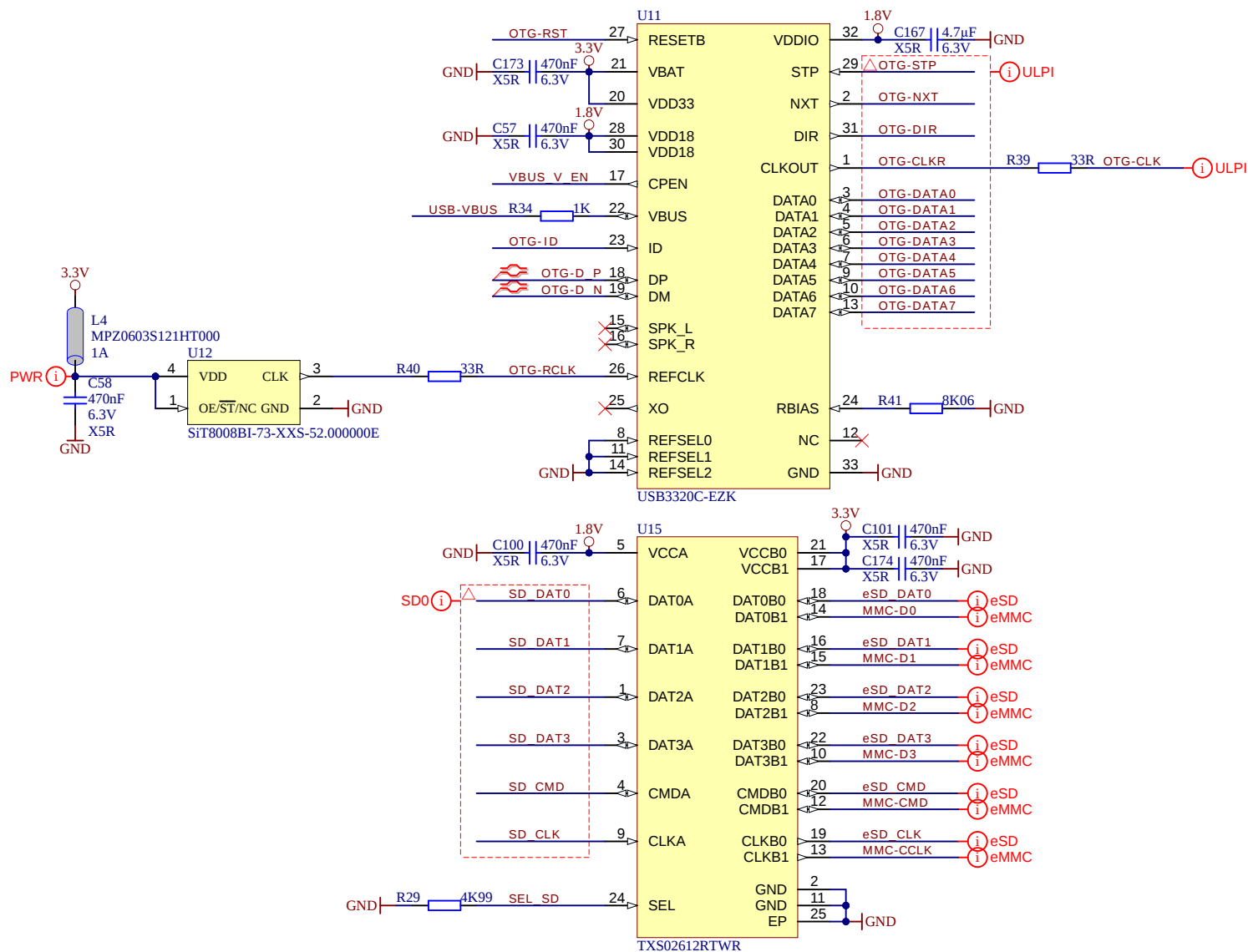
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Title: TE0729 – USB_PHY		
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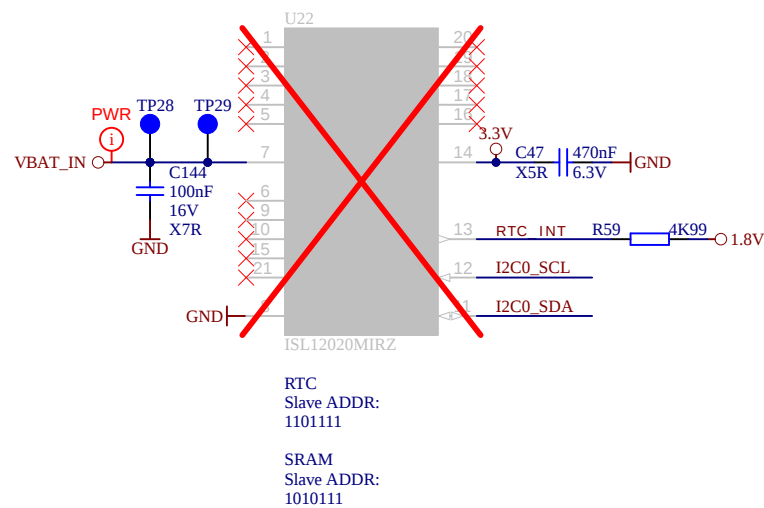
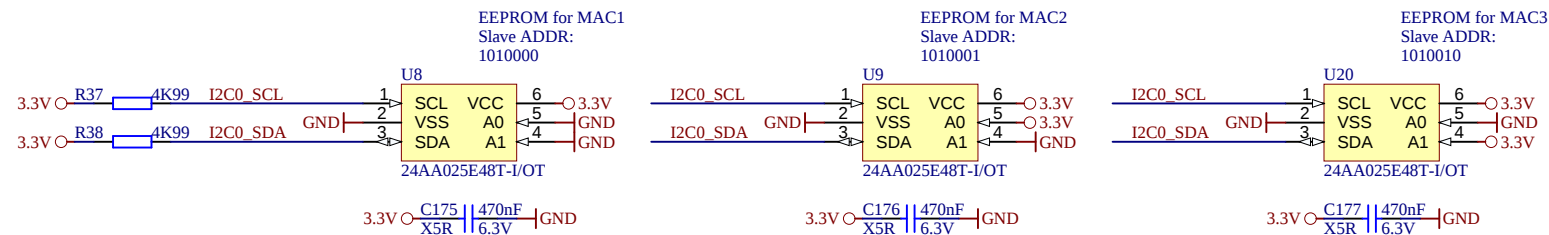
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Title: TE0729 – RTC		
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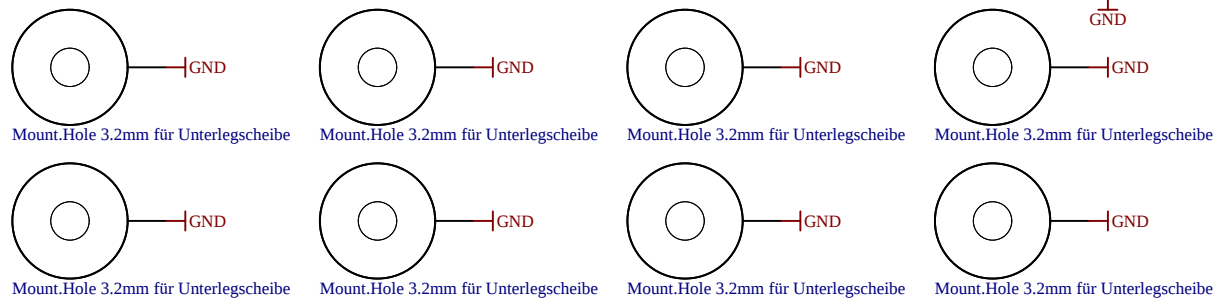
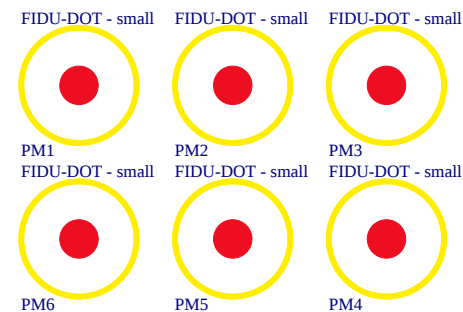
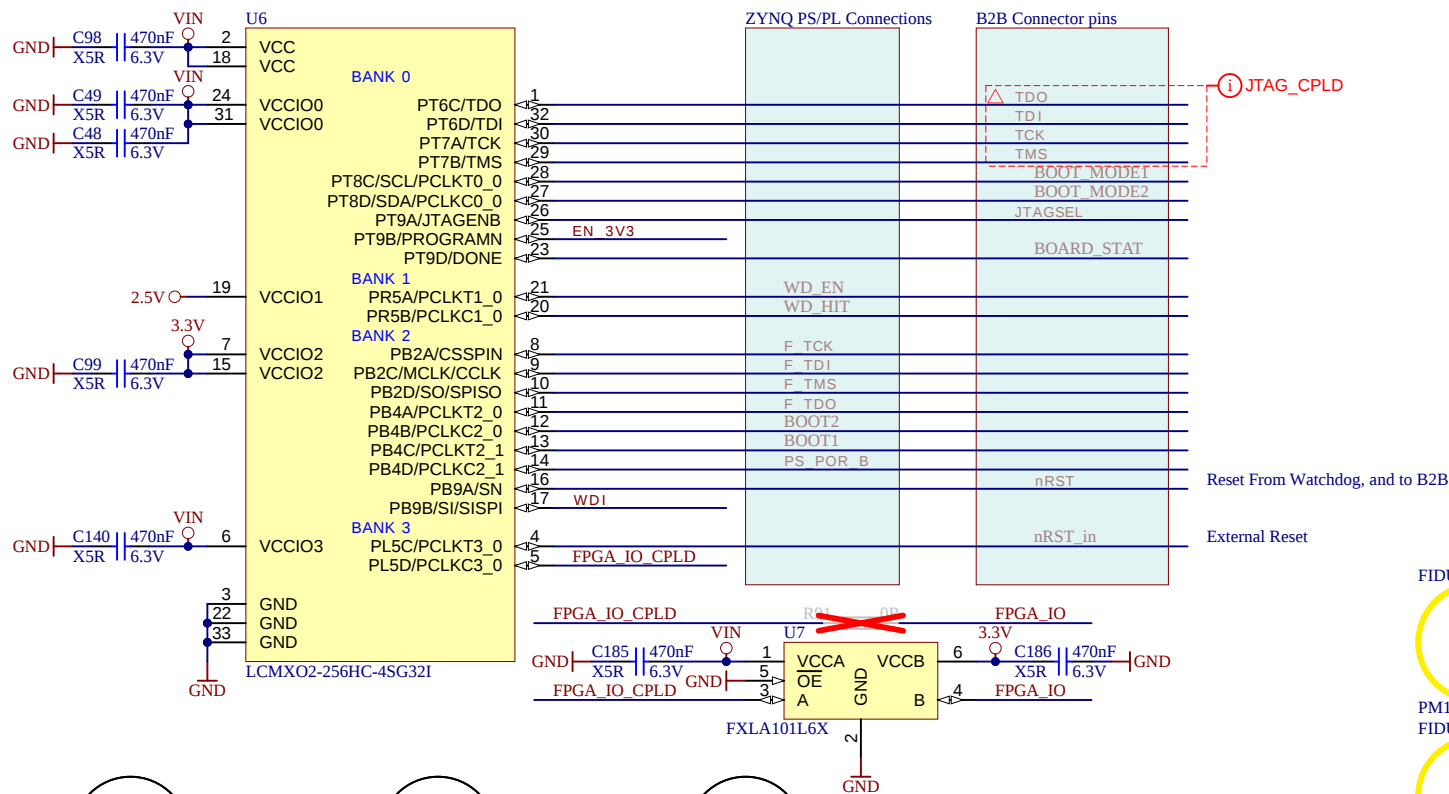
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Title: TE0729 – CPLD		
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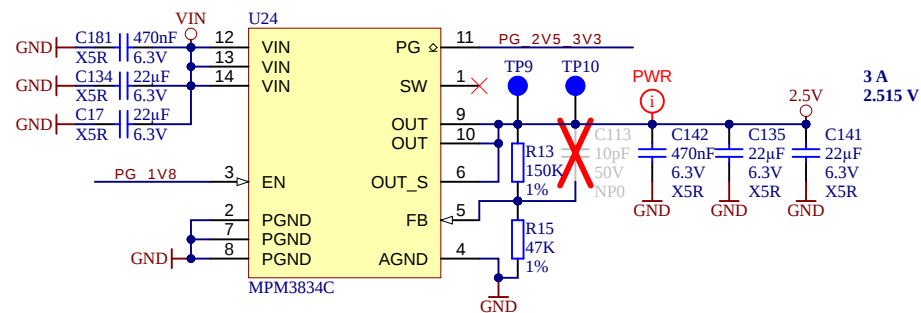
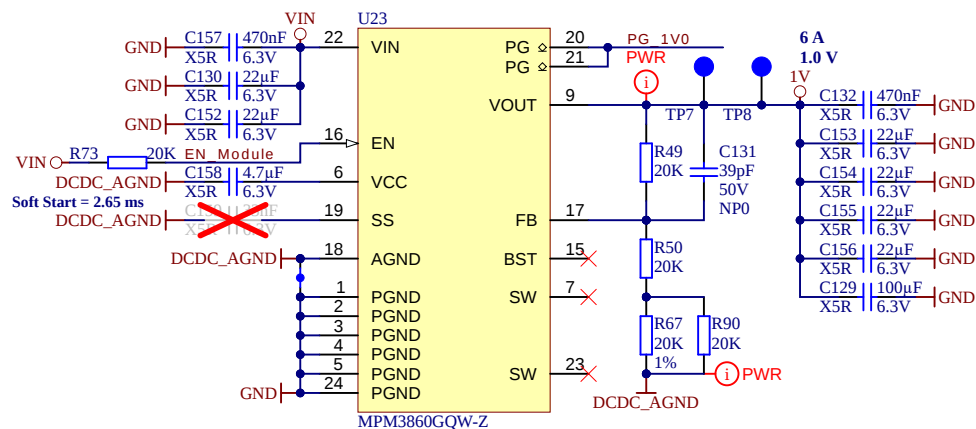
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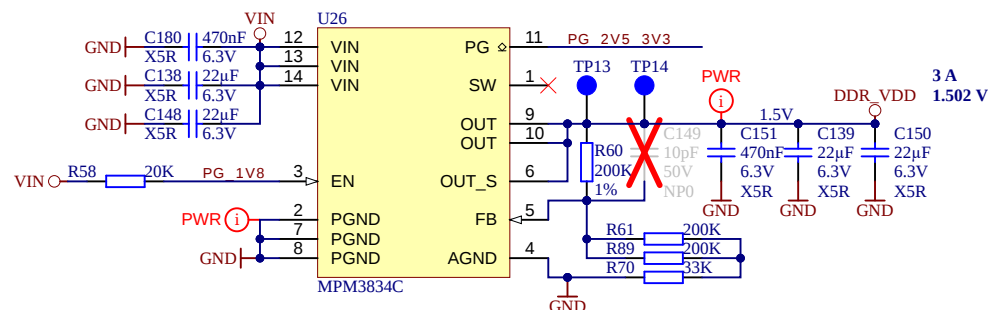
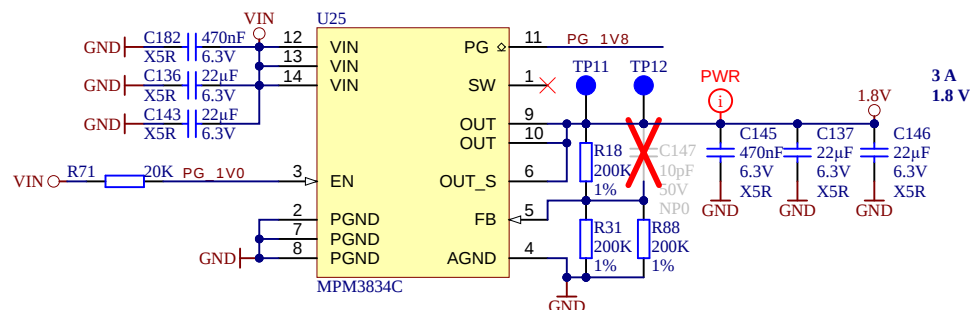
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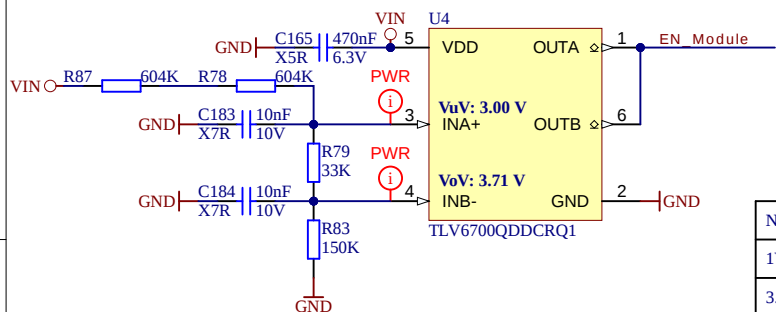
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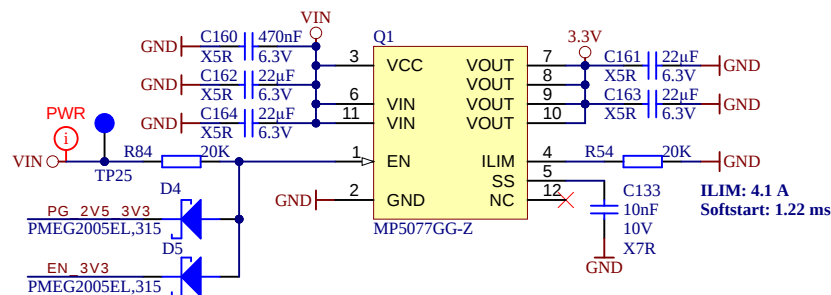
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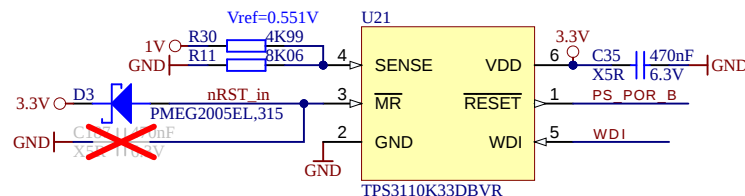
C



Net Name	Voltage Rail	Low Detect
1V	1.0 V	0.892 V
3.3V	3.3 V	2.941 V



D



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